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| 09/591,621 | 06/09/2000 | Vidyabhusan Gupta | 99-LJ-186 | 3053 |

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| EXAMINER | |
|---|---|
| DAY, HERNG DER | |
| **ART UNIT** | **PAPER NUMBER** |
| 2128 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/591,621 | GUPTA, VIDYABHUSAN | |
| | Examiner | Art Unit | |
| | Herng-der Day | 2128 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

**1.** This communication is in response to Applicant's Amendment and Response ("Amendment") to Office Action dated March 8, 2007, mailed July 9, 2007, and received by PTO July 16, 2007.

**1-1.** Claims 1 and 15-21 have been amended. Claims 1-29 are pending.

**1-2.** Claims 1-29 have been examined and rejected.

### *Claim Rejections - 35 USC § 102*

**2.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**3.** Claims 8-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Giorgi et al., "An Educational Environment for Program Behavior Analysis and Cache Memory Design", 1997 Frontiers in Education Conference, Proceedings of Teaching and Learning in an Era of Change, 1997, Volume 3, pages 1243-1248.

**3-1.** Regarding claim 8, Giorgi et al. disclose a method of designing a memory configuration for use in an embedded processing system, the method comprising the steps of:

simulating execution of a program to be executed by the embedded processing system (Applications can be executed and debugged on a dedicated ARM instruction set simulator, page 1244, left column, paragraph 3; cjpeg program, page 1246, right column, paragraph 2; cache

scheme defined by, for example, the mapping policy, the replacement algorithm, page 1245, right column, paragraph 2);

monitoring, during the simulated execution of the program, memory accesses to a simulated memory space (traces the execution of the cjpeg program, page 1246, right column, paragraph 2), wherein said memory accesses comprise read operations and write operations (read/write accesses, page 1244, left column, paragraph 5);

generating memory usage statistical data associated with the monitored memory accesses, (Analysis of Program Behavior, System Behavior, and Performance, page 1244, left column, paragraph 5 through right column, paragraph 2);

comparing the memory usage statistical data and one or more design criteria associated with the embedded processing system (for example, global system performance and cache behavior results from Performance Analysis, page 1244, right column, paragraph 2; for example, the image compression be completed in less than 1s, page 1246, right column, paragraph 2); and

in response to the comparison, determining at least one memory configuration capable of satisfying the one or more design criteria (select a configuration that best meets cost-effectiveness and performance requirements, page 1247, left column, paragraph 4, through page 1247, right column, paragraph 2).

**3-2.** Regarding claim 9, Giorgi et al. further disclose wherein the at least one memory configuration is determined from a set of memory types, the set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable

read-only memory (EEPROM) (for example, a 1-Mbyte memory DRAM bank, a 128-Kbyte memory PROM bank, page 1246, right column, paragraph 3).

**3-3.** Regarding claim 10, Giorgi et al. further disclose wherein the at least one memory configuration comprises a first memory type and a first memory size associated with the first memory type (For each module, the configuration parameters include the module type, the starting address and the size, page 1246, right column, paragraph 7).

**3-4.** Regarding claim 11, Giorgi et al. further disclose wherein the at least one memory configuration further comprises a second memory type and a second memory size associated with the second memory type (For each module, the configuration parameters include the module type, the starting address and the size, page 1246, right column, paragraph 7).

**3-5.** Regarding claim 12, Giorgi et al. further disclose wherein the step of simulating execution of the program comprises the sub-steps of simulating execution of the program N times, wherein the step of monitoring the memory accesses comprises the sub-steps of monitoring the memory accesses during the N simulated executions of the program, and wherein the step of generating the memory usage statistical data is based on the N simulated executions of the program (trace analysis, page 1244, left column, paragraph 5; allows the cache to exit its cold state and to reach a steady condition, page 1244, right column, paragraph 2).

**3-6.** Regarding claim 13, Giorgi et al. further disclose comprising the step of determining at least one figure of merit associated with the at least one memory configuration, wherein the at least one figure of merit indicates a degree to which the at least one memory configuration satisfies the one or more design criteria (for example, max delay as shown in Table 1 at page 1248 can be used as figure of merit to select a configuration for rawcaudio program).

**3-7.** Regarding claim 14, Giorgi et al. further disclose comprising the step of modifying the program in response to the comparison of the memory usage statistical data and the one or more design criteria to thereby enable the embedded processing system to execute the program according to the one or more design criteria (cache scheme defined by, for example, the mapping policy, the replacement algorithm, page 1245, right column, paragraph 2).

**3-8.** Regarding claims 15-21, these system claims include equivalent method limitations as in claims 8-14 and are anticipated using the same analysis of claims 8-14.

**3-9.** Regarding claims 22-28, these medium claims include equivalent method limitations as in claims 8-14 and are anticipated using the same analysis of claims 8-14.

### *Claim Rejections - 35 USC § 103*

**4.** The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**5.** Claims 1-7 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giorgi et al., "An Educational Environment for Program Behavior Analysis and Cache Memory Design", 1997 Frontiers in Education Conference, Proceedings of Teaching and Learning in an Era of Change, 1997, Volume 3, pages 1243-1248, in view of MPEP 2144.04(III) routine expedients of automating a manual activity.

**5-1.** Regarding claim 1, Giorgi et al. disclose an apparatus for designing a memory configuration for use in an embedded processing system comprising:

[a simulation controller capable of] simulating execution of a program to be executed by said embedded processing system (Applications can be executed and debugged on a dedicated ARM instruction set simulator, page 1244, left column, paragraph 3; cjpeg program, page 1246, right column, paragraph 2; cache scheme defined by, for example, the mapping policy, the replacement algorithm, page 1245, right column, paragraph 2);

[a memory access monitor capable of] monitoring, during said simulated execution of said program, memory accesses to a simulated memory space (traces the execution of the cjpeg program, page 1246, right column, paragraph 2), [wherein said memory access monitor is capable of] generating memory usage statistical data associated with said monitored memory accesses (Analysis of Program Behavior, System Behavior, and Performance, page 1244, left column, paragraph 5 through right column, paragraph 2), and wherein said memory accesses comprise read operations and write operations (read/write accesses, page 1244, left column, paragraph 5); and

[a memory optimization controller capable of] comparing said memory usage statistical data and one or more design criteria associated with said embedded processing system (for example, global system performance and cache behavior results from Performance Analysis, page 1244, right column, paragraph 2; for example, the image compression be completed in less than 1s, page 1246, right column, paragraph 2) and, in response to said comparison, determining at least one memory configuration capable of satisfying said one or more design criteria (select a configuration that best meets cost-effectiveness and performance requirements, page 1247, left column, paragraph 4, through page 1247, right column, paragraph 2).

Giorgi et al. fail to expressly disclose the simulation controller, memory access monitor, and memory optimization controller. However, this limitation is disclosed by MPEP 2144.04(III) routine expedients of automating a manual activity. In re Venner, 262 F.2d 91, 95, 120 USPQ 193, 194 (CCPA 1958). The court held that broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art. In this claim, as described in the specification at page 7, lines 10-13, and page 11, lines 11-15, the simulation controller, memory access monitor, and memory optimization controller may all be implemented as memory design and optimization application programs where the functions of simulating, monitoring, comparing, determining, and so on are performed following a programmed sequence to replace manual activities, however, still accomplished the same result. Therefore, incorporating the software controllers, etc., is obvious and not contrary to the understandings and expectations of the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Giorgi et al. to incorporate the legal precedent teachings of automating a manual activity to obtain the invention as specified in claim 1 because it is considered to be a routine expedient.

**5-2.** Regarding claim 2, Giorgi et al. further disclose said at least one memory configuration is determined from a set of memory types, said ' set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM) (for example, a 1-Mbyte memory DRAM bank, a 128-Kbyte memory PROM bank, page 1246, right column, paragraph 3).

**5-3.** Regarding claim 3, Giorgi et al. further disclose said at least one memory configuration comprises a first memory type and a first memory size associated with said first memory type (For each module, the configuration parameters include the module type, the starting address and the size, page 1246, right column, paragraph 7).

**5-4.** Regarding claim 4, Giorgi et al. further disclose said at least one memory configuration further comprises a second memory type and a second memory size associated with said second memory type (For each module, the configuration parameters include the module type, the starting address and the size, page 1246, right column, paragraph 7).

**5-5.** Regarding claim 5, Giorgi et al. further disclose said simulation controller simulates execution of said program N times and wherein said memory access monitor monitors said memory accesses during said N simulated executions of said program and generates said memory usage statistical data based on said N simulated executions of said program (trace analysis, page 1244, left column, paragraph 5; allows the cache to exit its cold state and to reach a steady condition, page 1244, right column, paragraph 2).

**5-6.** Regarding claim 6, Giorgi et al. further disclose said memory optimization controller is further capable of determining at least one figure of merit associated with said at least one memory configuration, wherein said at least one figure of merit indicates a degree to which said at least one memory configuration satisfies said one or more design criteria (for example, max delay as shown in Table 1 at page 1248 can be used as figure of merit to select a configuration for rawcaudio program).

**5-7.** Regarding claim 7, Giorgi et al. further disclose comprising a code optimization controller capable of modifying said program in response to said comparison of said memory

usage statistical data and said one or more design criteria to thereby enable said embedded processing system to execute said program according to said one or more design criteria (cache scheme defined by, for example, the mapping policy, the replacement algorithm, page 1245, right column, paragraph 2).

**5-8.** Regarding claim 29, Giorgi et al. further disclose the memory usage statistical data comprises at least one of:

one or more first histograms based on variable names contained in the program to be executed by the embedded processing system; and one or more second histograms based on memory locations accessed by the program to be executed by the embedded processing system (page 1245, Figure 2).

***Applicant's Arguments***

**6.** Applicant argues the following:

**6-1.** REJECTION UNDER 35 U.S.C. § 112

(1) "Applicant has amended these claims to recite that the embedded processing system comprises a memory configuration designed according to the method as set forth [in a previous claim]. Therefore, Applicant respectfully submits these claims are definite." (Pages 10-11, Amendment).

**6-2.** REJECTION UNDER 35 U.S.C. § 101

(2) "Applicant has amended Claim 1 to recite the apparatus comprises a processing system which comprises the other recited elements." (Page 11, paragraph 4, Amendment).

**6-3.** REJECTION UNDER 35 U.S.C. § 102

(3) "Applicant reiterates, and incorporates by reference herein, its responses, arguments and reasoning as set forth in Applicant's Appeal Brief filed November 13, 2006 (and prior responses) with respect to the 102 rejection of Claims 8-28." (Page 12, paragraph 2, Amendment).

**6-4.** REJECTION UNDER 35 U.S.C. § 103

(4) "Applicant reiterates, and incorporates by reference herein, its responses, arguments and reasoning as set forth in Applicant's Appeal Brief filed November 13, 2006 (and prior responses) with respect to Claims 1-7 and 29." (Page 12, paragraph 5, Amendment).

(5) "Giorgi does not disclose each and every element/feature - either structurally or functionally (or results) - as recited in independent Claim 1. Therefore, the Office's citation to the MPEP (and In re Venner) is irrelevant - as the Office has failed to establish that Giorgi teaches all of the functional elements/features recited in Claim 1. ... Applicant submits that its apparatus accomplishes a different result than Giorgi. Thus, In re Venner is inapplicable." (Page 13, paragraph 2, Amendment).

***Response to Arguments***

**7.** Applicant's arguments have been fully considered.

**7-1.** Applicant's argument (1) is persuasive. The rejections of claims 15-21 under 35 U.S.C. 112, second paragraph, in Office Action dated March 8, 2007, have been withdrawn.

**7-2.** Applicant's argument (2) is persuasive. The rejections of claims 1-7 and 29 under 35 U.S.C. 101 in Office Action dated March 8, 2007, have been withdrawn.

**7-3.** Applicant's arguments (3) and (4) are not persuasive. Applicant reiterates, and incorporates by reference herein, its responses, arguments and reasoning as set forth in Applicant's Appeal Brief filed November 13, 2006, without new arguments. All the arguments as set forth in Applicant's Appeal Brief have been responded in Office Action dated March 8, 2007.

**7-4.** Applicant's argument (5) is not persuasive. Applicant merely argues its apparatus accomplishes a different result than Giorgi without providing any evidence or point out the difference.

***Conclusion***

**8.** **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**9.** Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
October 1, 2007 H.D.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER